REMARKS

The specification has been amended to conform it to the filed drawings (i.e., FIG. 10A).

Claims 3-5, 8-10, 12, 15, 17, 19, 22, 25, 27, 28 and 30 have been amended, claims 31-35 have been added, and claims 1, 2, 7, 11, 16, 18, 22, 26, and 29 have been canceled. Claims 3-6, 8-10, 12-15, 17, 19-25, 27, 28, and 30-35 remain in the application.

In the Office Action of July 5, 2006, the Examiner stated that claims 3, 9, 15, 19, 22 and 27 would be allowable if rewritten in independent form.

Accordingly, Applicant has amended claim 3 to be in independent form including the limitations of claims 1 and 2 which have been canceled. Claims 4 and 5 have been amended to depend from now-independent claim 3, claim 6 remains dependent from claim 5, and claim 7 has been canceled.

In addition, Applicant has amended claim 9 to be in independent form including the limitations of claims 1 and 2. Claims 8 and 10 have been amended to depend from now-independent claim 9.

In addition, Applicant has amended claim 15 to be in independent form including the limitations of claims 11, 16, and 18 which have been canceled. Claims 12 and 17 have been amended to depend from now-independent claim 15 and claims 13 and 14 remain depended from claim 12.

In addition, Applicant has amended claim 19 to be in independent form including the limitations of claim 18. Claim 20 remains depended from claim 19 and claim 21 remains dependent from claim 20.

In addition, Applicant has amended claim 22 to be in independent form including the limitations of claim 18. Claims 23 and 24 remain depended from claim 22 and claim 25 has been amended to depend from claim 22.

Finally, Applicant has amended claim 27 to be in independent form including the limitations of claims 26 and 29. Claims 28 and 30 have been amended to depend from claim 27.

Applicants have added claims 31-35. Independent claim 31 recites a reference generator that includes an oscillator and a buffer amplifier that provide a reference signal wherein the buffer amplifier's gain corresponds to a gain-control signal. In addition, claim 31 recites a low-pass filter, a string of resistors, and an input differential pair of transistors.

As further recited in claim 31, the low-pass filter extracts a common-mode level from the reference signal, the string of resistors defines upper and lower tap points and a junction between the upper and lower tap points, and the input differential pair of transistors have an output coupled to drive the string and have a differential input coupled between the filter and the junction to thereby transfer the common-mode level to the junction.

Claim 31 then recites upper and lower differential pairs of transistors that generate first and second pulse trains in response to their differential inputs which are coupled between the reference signal and selected ones of the upper and lower tap points.

Accordingly, this recited structure receives a reference signal and forms, from this reference signal, a common-mode signal which is then translated up and down to selected tap points. The upper and lower differential pairs then compare the reference signal to the translated common-mode signals at these tap points to thereby generate pulse trains which are applied to a counter whose count comprises a gain-control signal at the buffer amplifier. The count continues until the first and second pulse trains cease.

It is important to note that the upper and lower differential pairs do not compare the reference signal to an external signal that is brought in for this purpose. Rather, they compare the reference signal to signals at tap points that have been translated up and down from a common-mode signal which is derived from the reference signal itself.

The Examiner has previously referred to teachings of **Cho** (U.S. Patent No. 6,917,229). As shown in his FIG. 2, Cho provides a delay line 250 to convert a reference clock signal into a delayed (dll) clock signal. Cho teaches that the dll clock signal should be compared in a phase detector with the reference clock

signal to obtain an UP/DN signal which is then applied to an up/down counter 244 and signals from the up/down counter are applied as control signals to the delay line 250. Thus, Cho teaches that the output of his delay line must be compared to an external signal (the reference clock) to generate a signal for application to his up/down counter. This can be more easily seen in Cho's FIG. 1 where the output of his delay line 140 is compared in his phase detector 120 to an external signal (clock) in order to provide a comparison signal to his counter 130.

As noted above, Applicants' claim 31 does not follow this teaching because it compares the output of its buffer amplifier to translations of a common-mode signal which is derived from the buffer amplifier output. That is, Applicants' claim 31 does not compare the output of its buffer amplifier to any external signal but, rather, to a signal derived from the output itself. Applicants' claim 31 thus recites structure which loops from the amplifier output back to the amplifier's gain-control signal and no external signal is introduced into this looped structure.

Because Cho fails to teach the structure of Applicants' claim 31, he cannot anticipate this structure. Because Cho, in fact, teaches away from this structure, he cannot contribute to a *prima facie* case of obviousness with respect to this structure. Claim 31 thus patentably distinguishes over Cho and because claims 32-35 add further limitations to claim 31, they also patentably distinguish over Cho.

Applicants therefore request an early allowance of claims 3-6, 8-10, 12-15, 17, 19-25, 27, 28 and 30-35.

Respectfully submitted,
Marc E. Goldfarb
Edmund J. Balboni

By _____
Joseph Compton
Registration No. 34,308

KOPPEL, PATRICK & HEYBL
555 St. Charles Drive, Suite 107
Thousand Oaks, CA 91360
(818) 788-6983